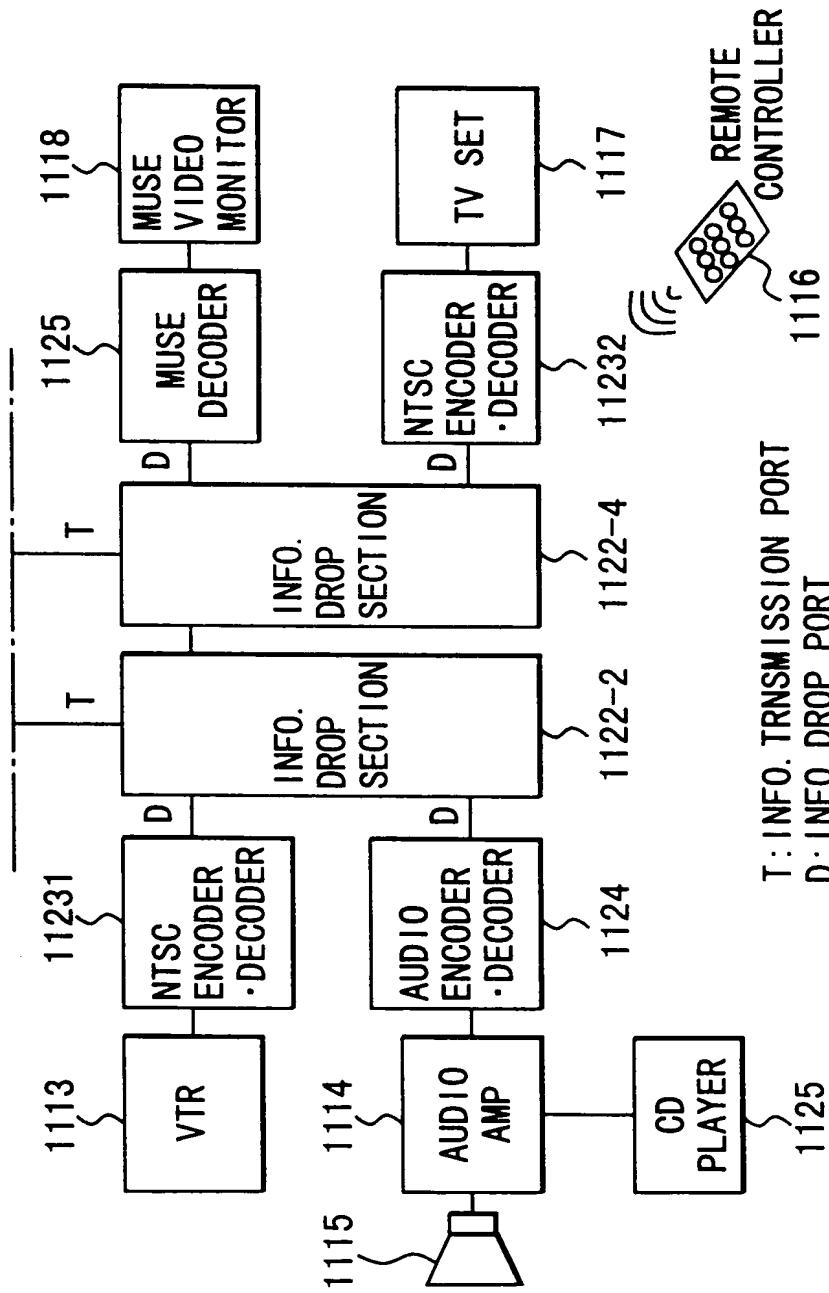


FIG. 1 A



F I G . 1 B

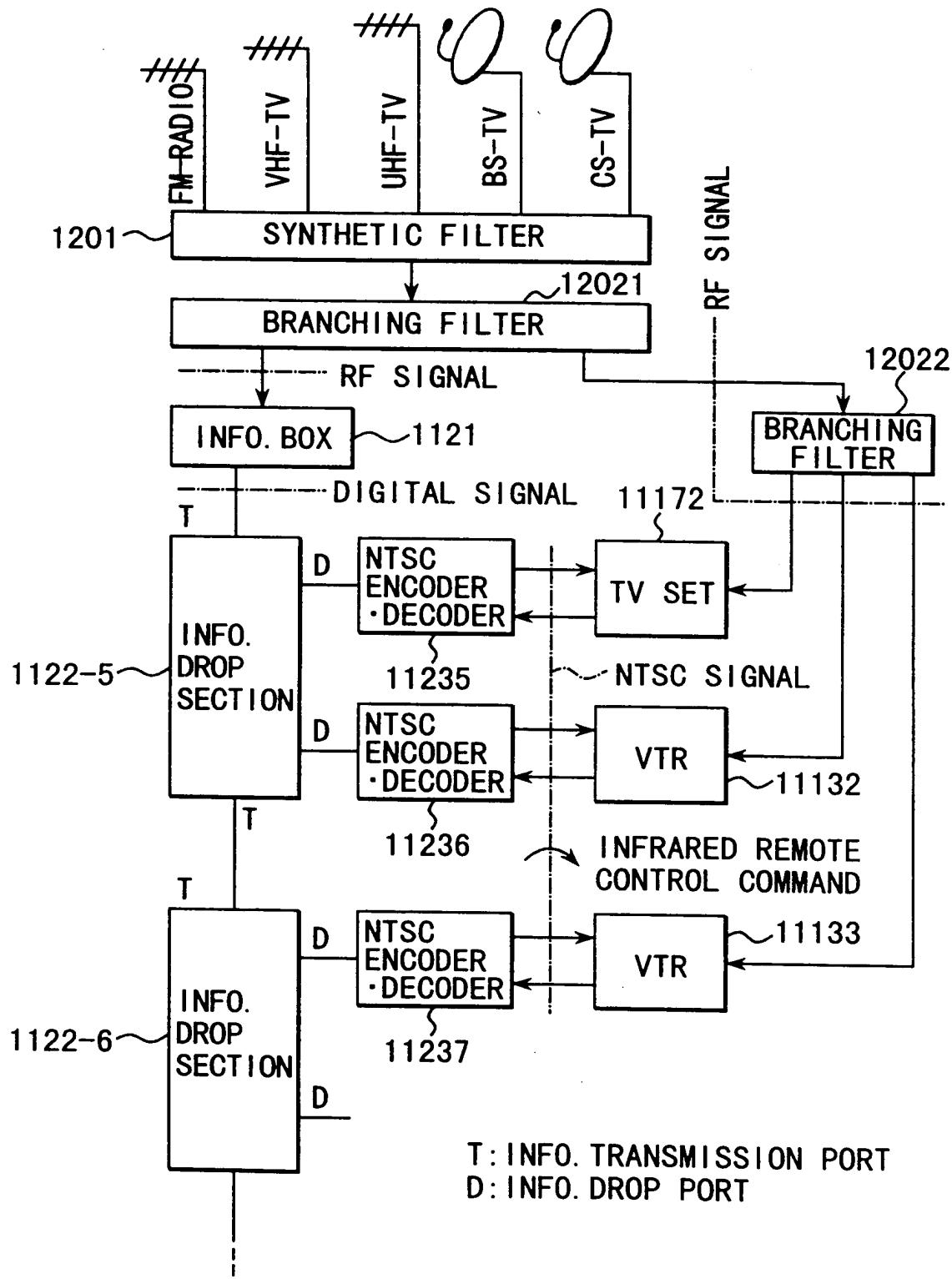


FIG. 2

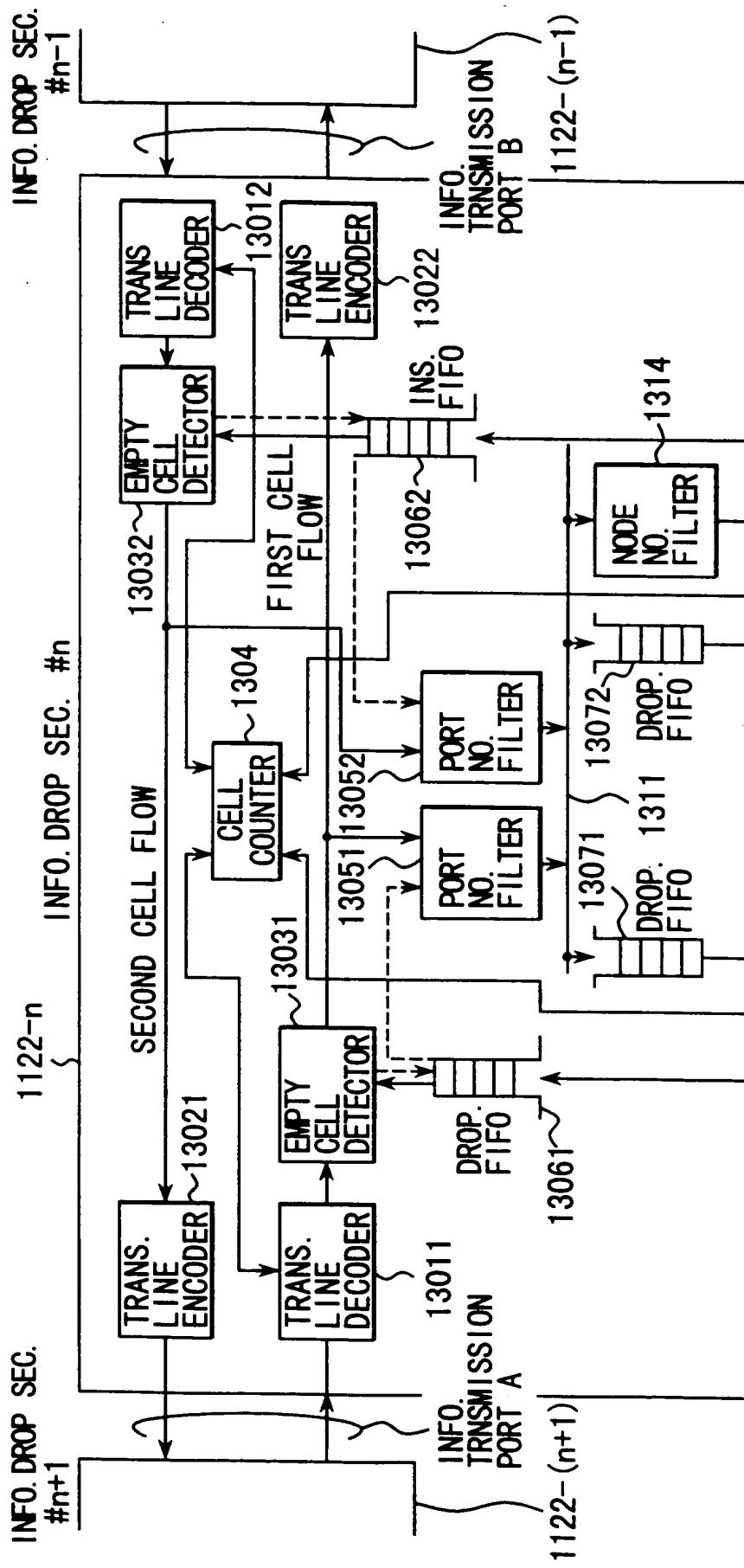


FIG. 3A

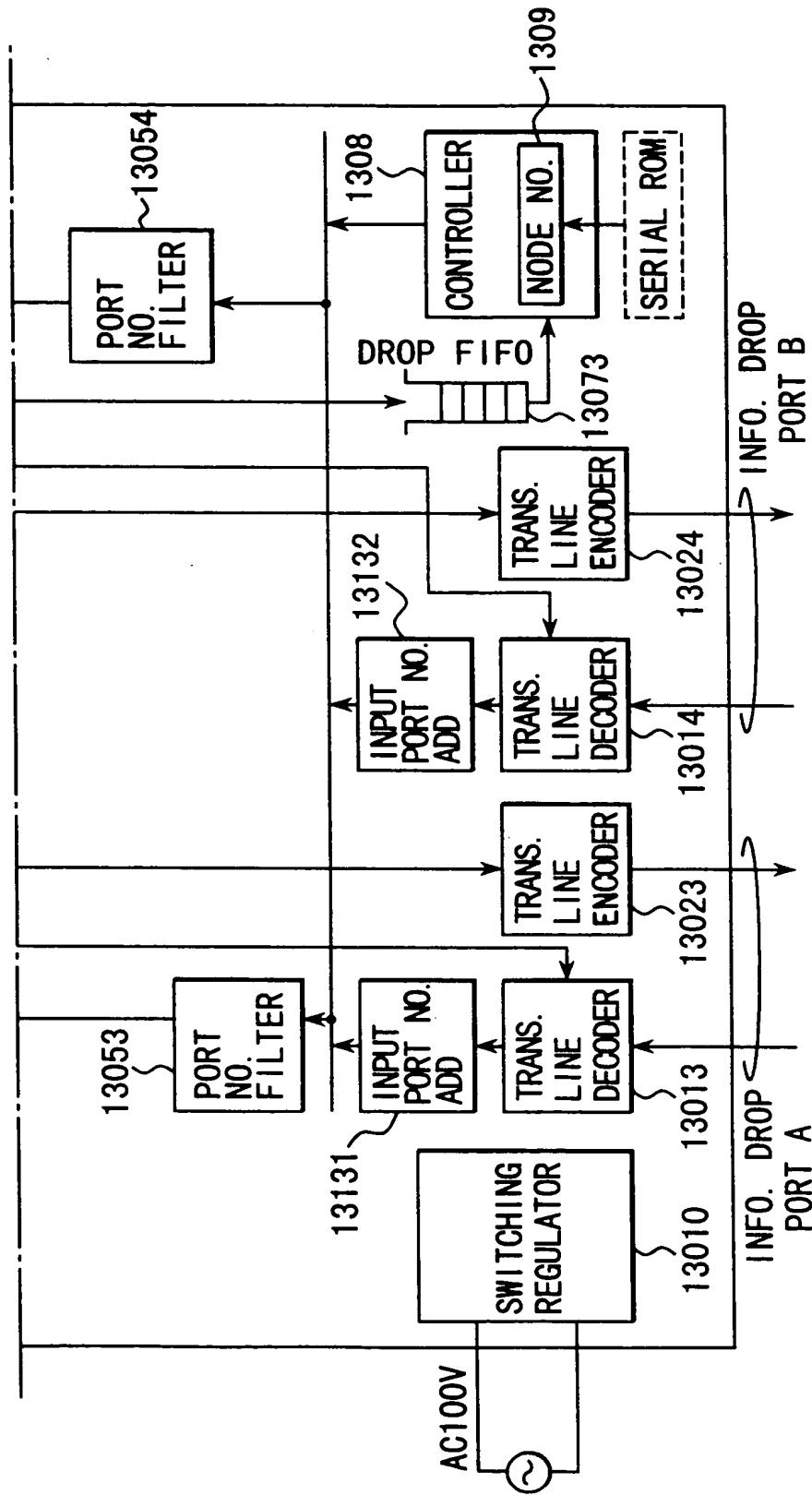
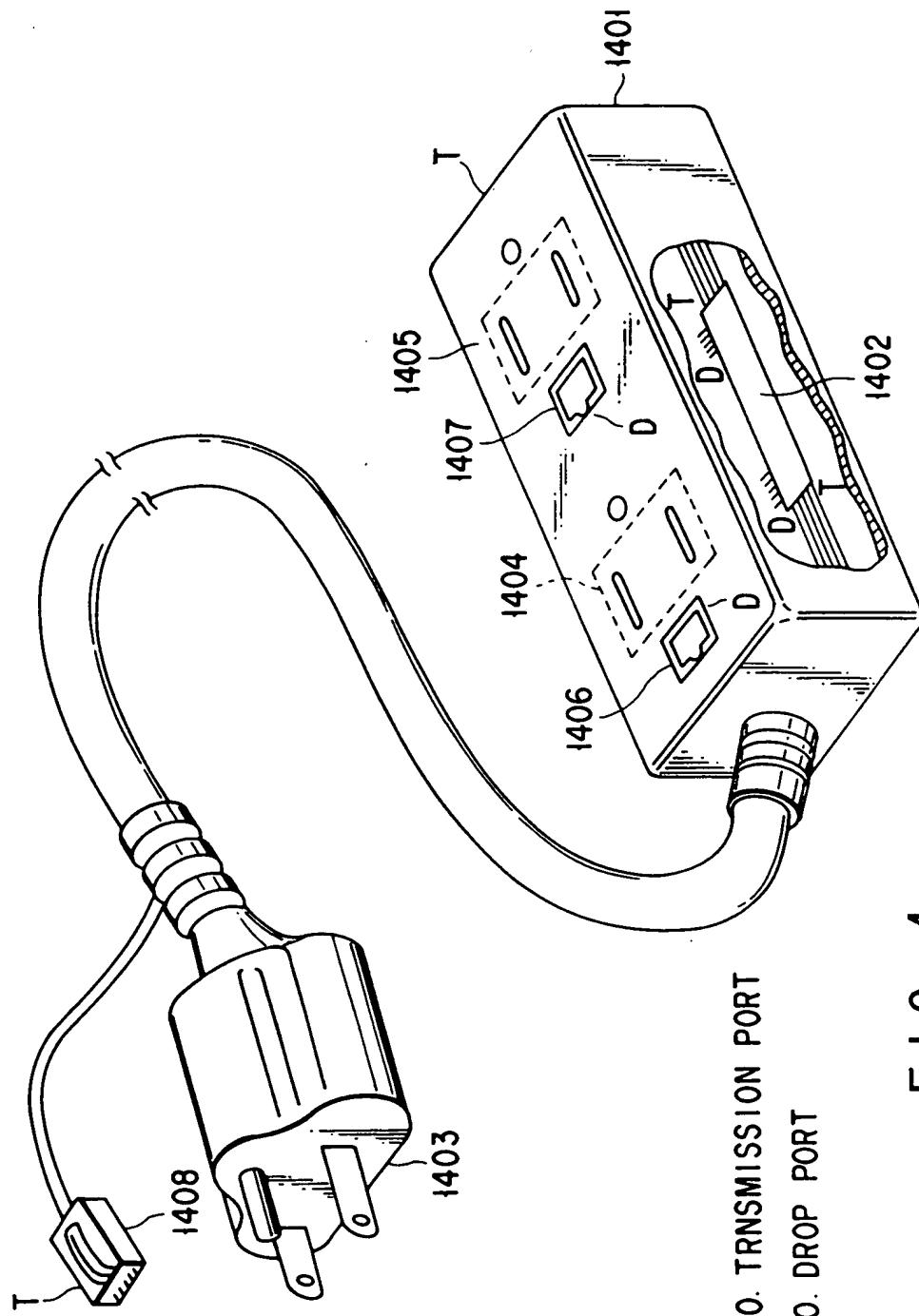
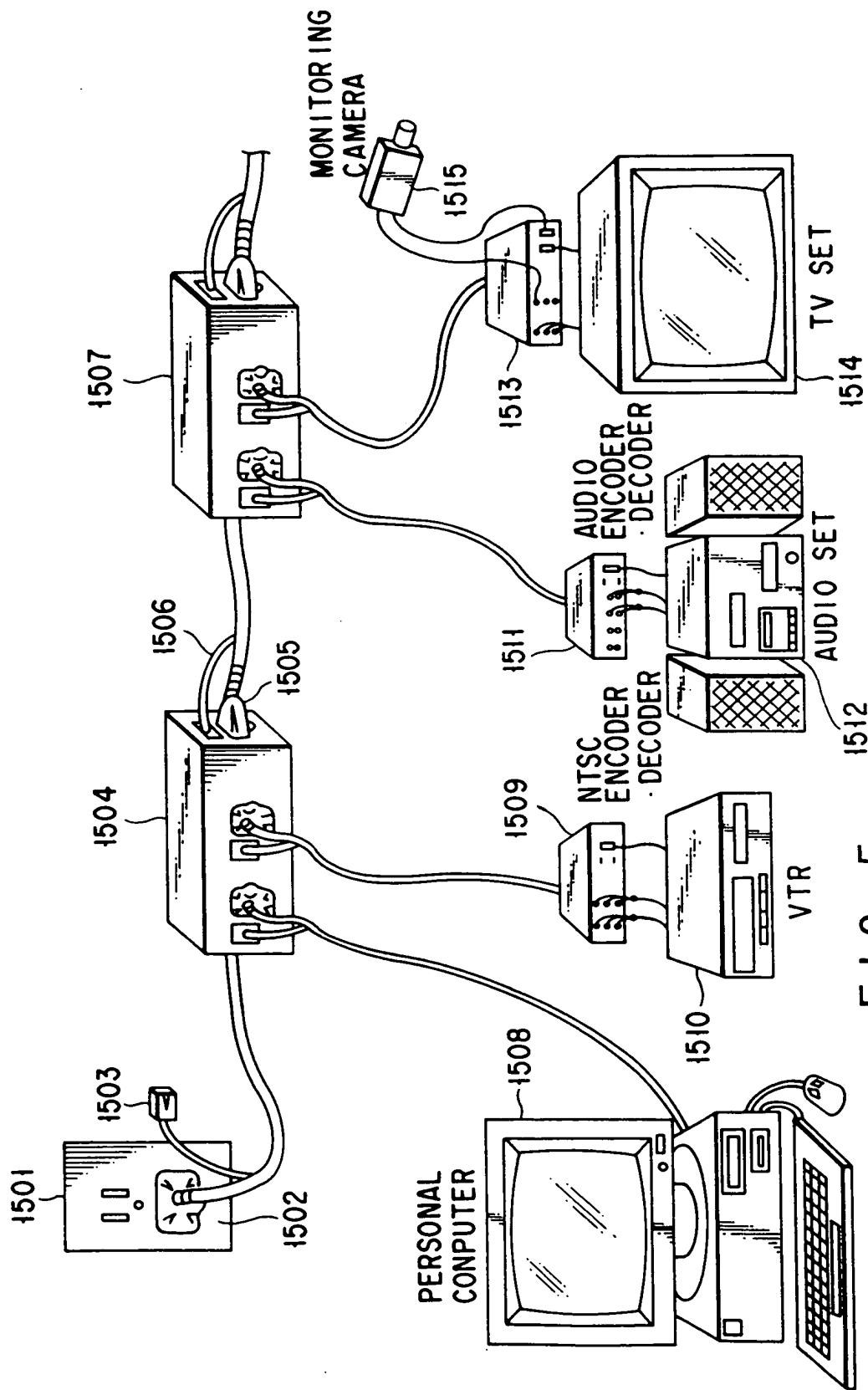


FIG. 3B



T: INFO. TRANSMISSION PORT
D: INFO. DROP PORT

F I G . 4



F I G . 5

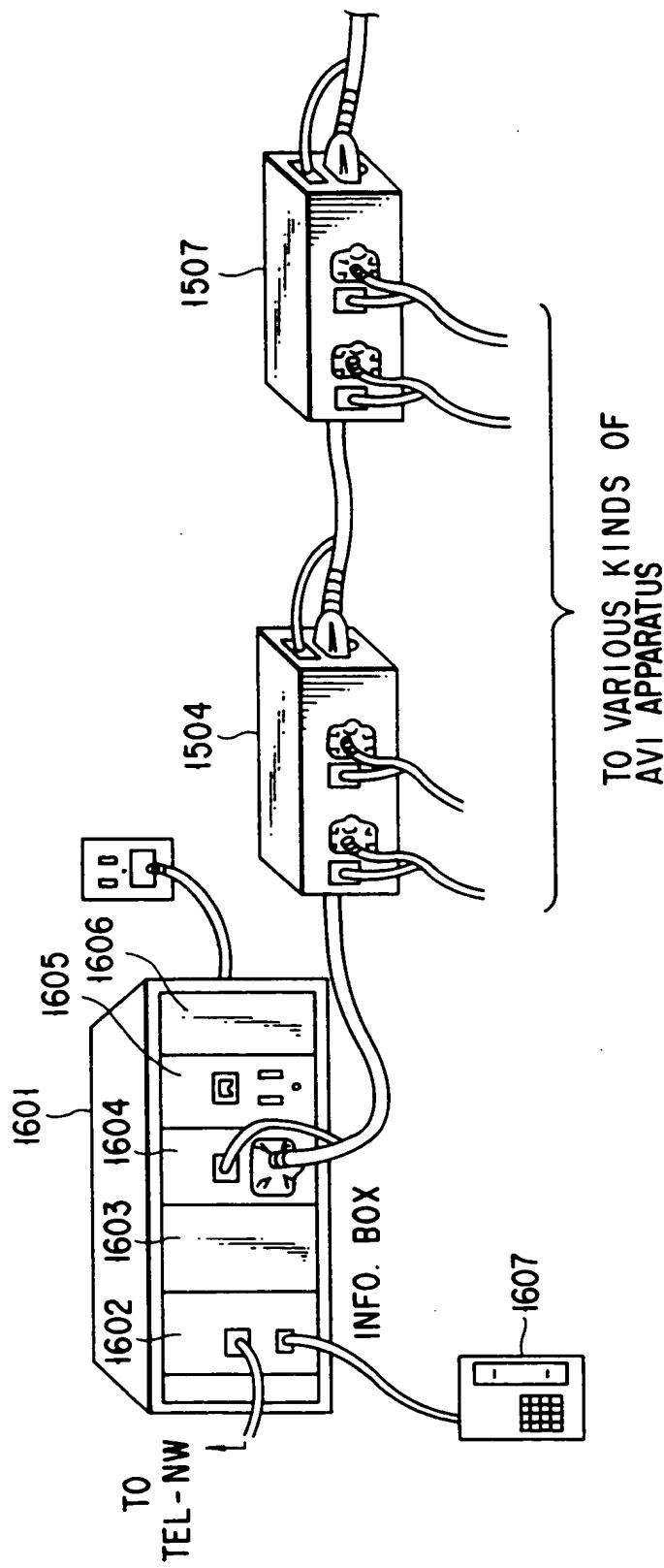
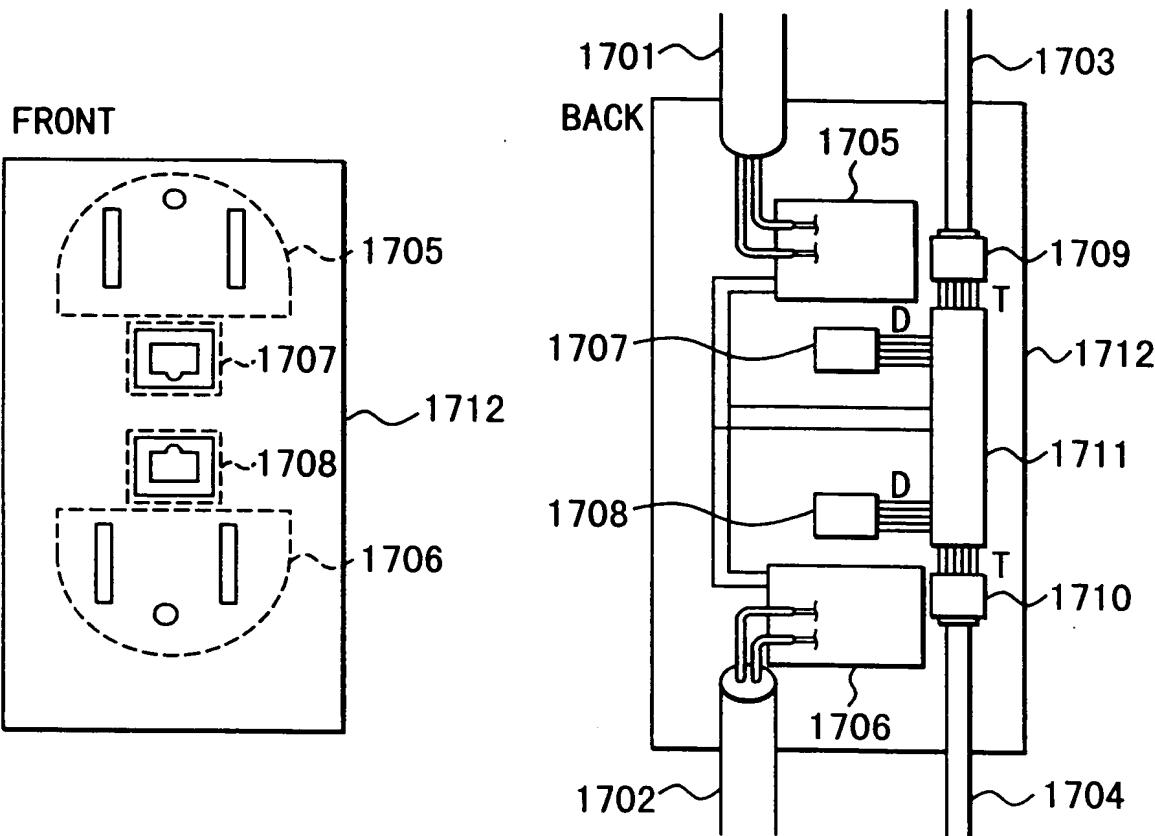
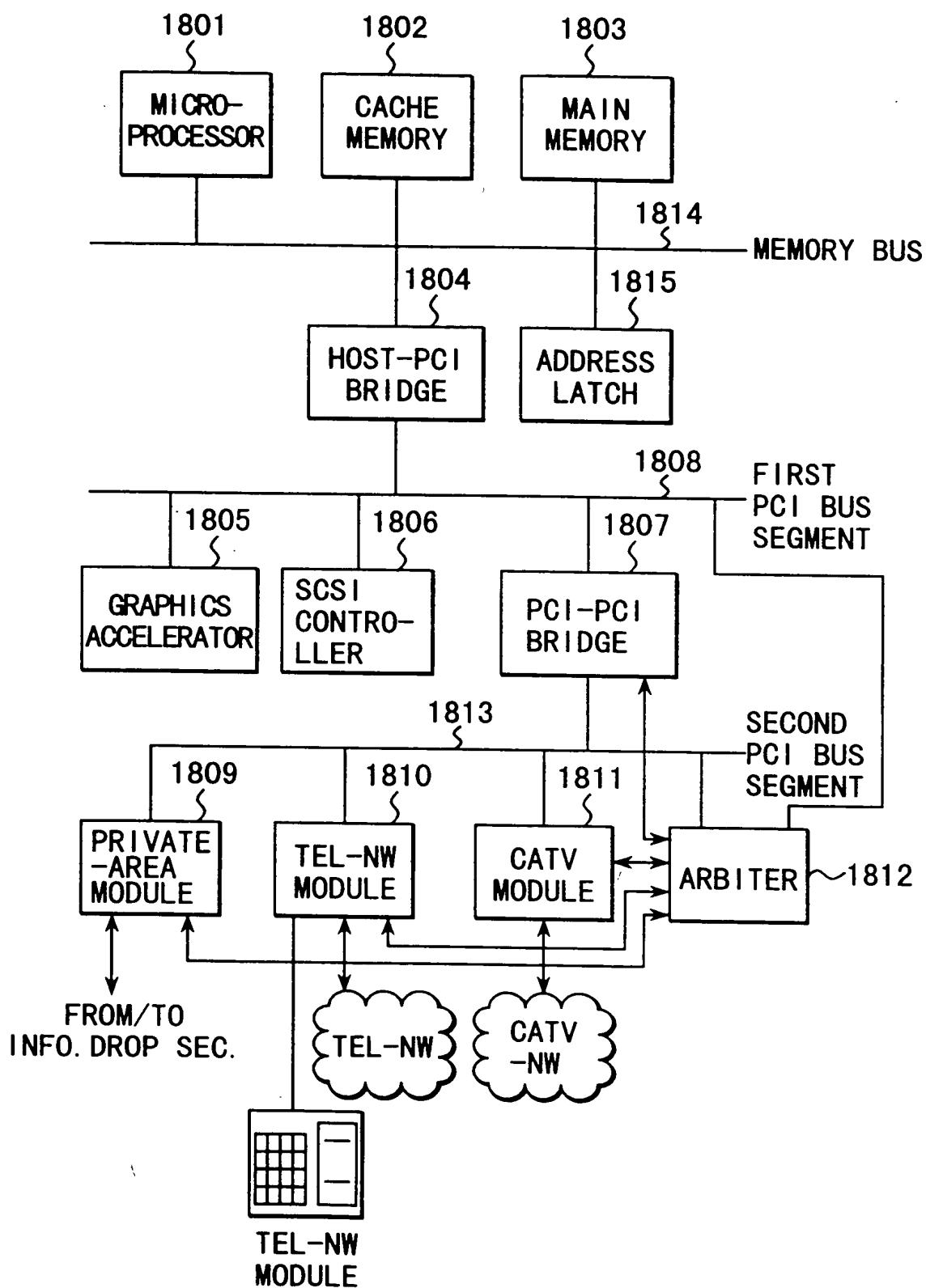


FIG. 6

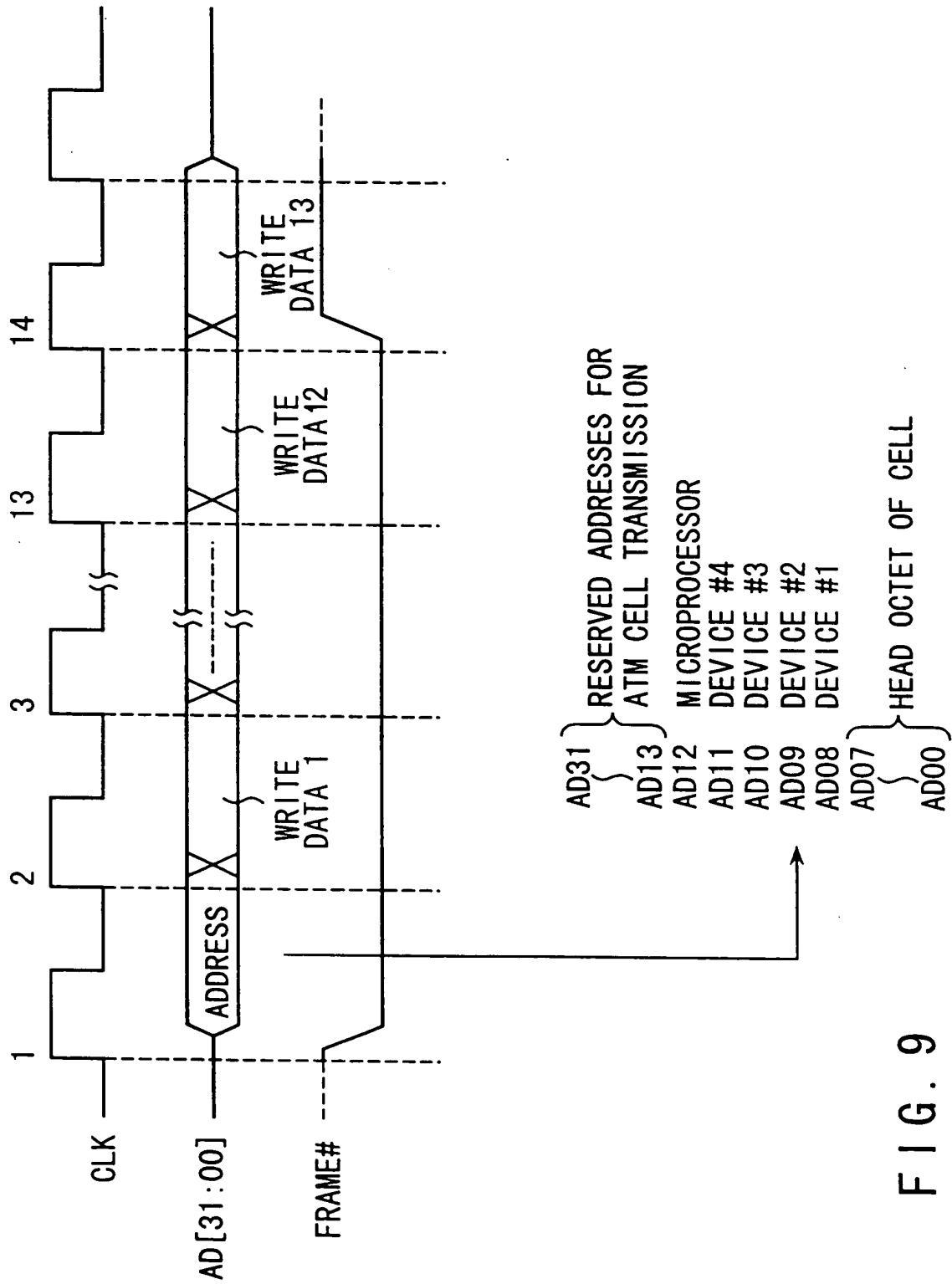


T: INFO. TRANSMISSION PORT
D: INFO. DROP PORT

FIG. 7



F I G . 8



F I G. 9

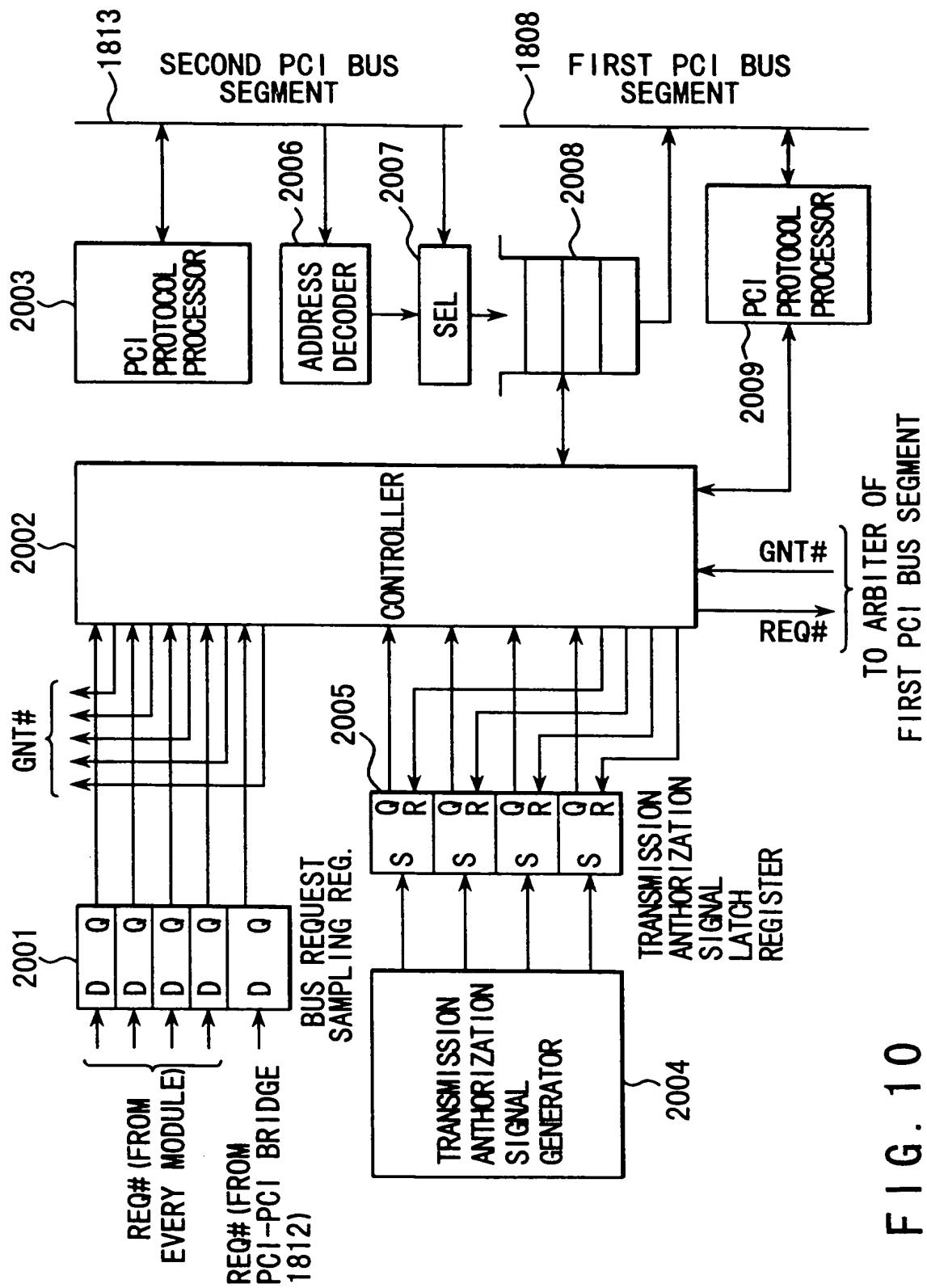


FIG. 10
 TO ARBITER OF
 FIRST PCI BUS SEGMENT

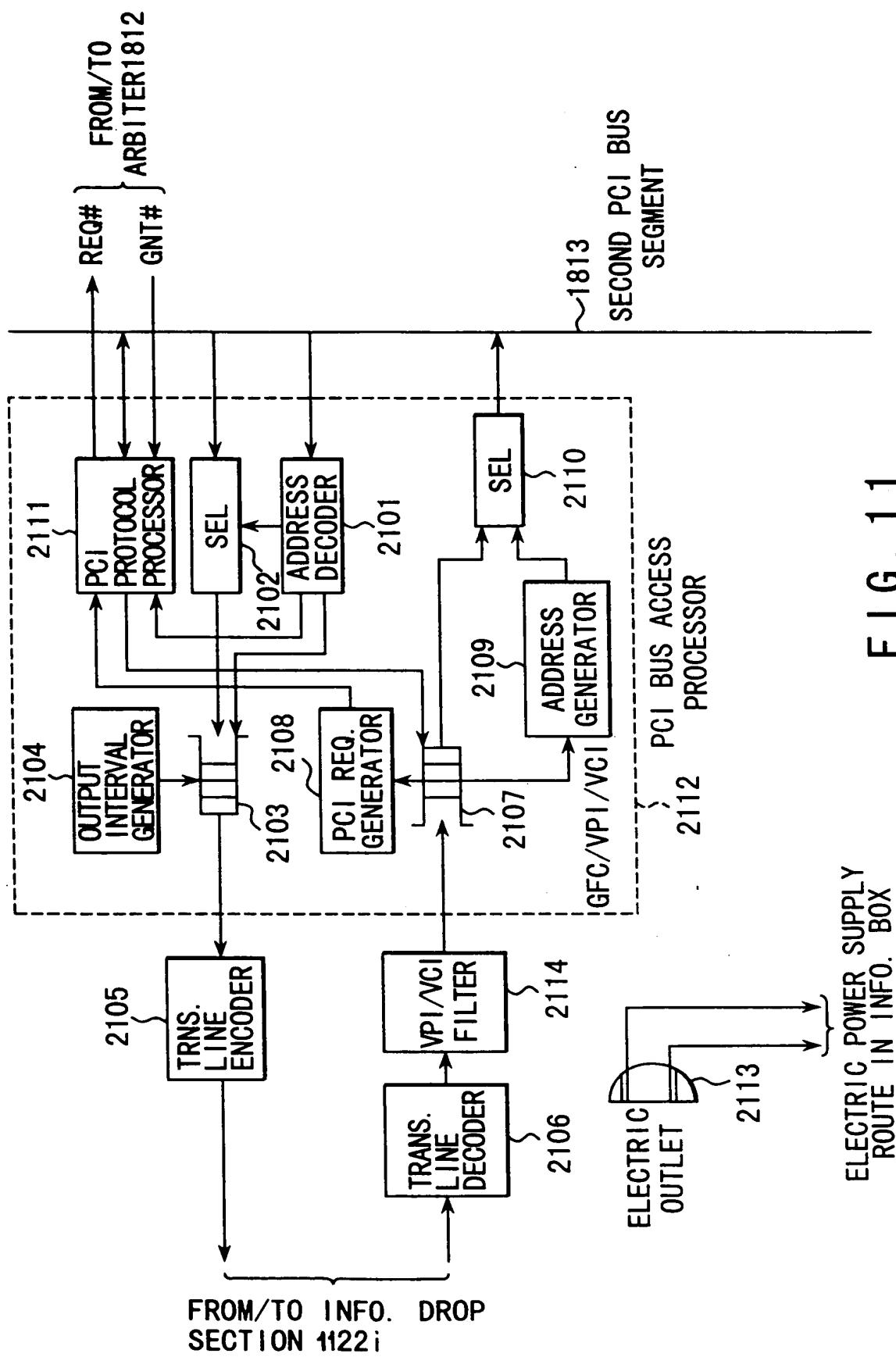


FIG. 11

ELECTRIC POWER SUPPLY
 ROUTE IN INFO. BOX

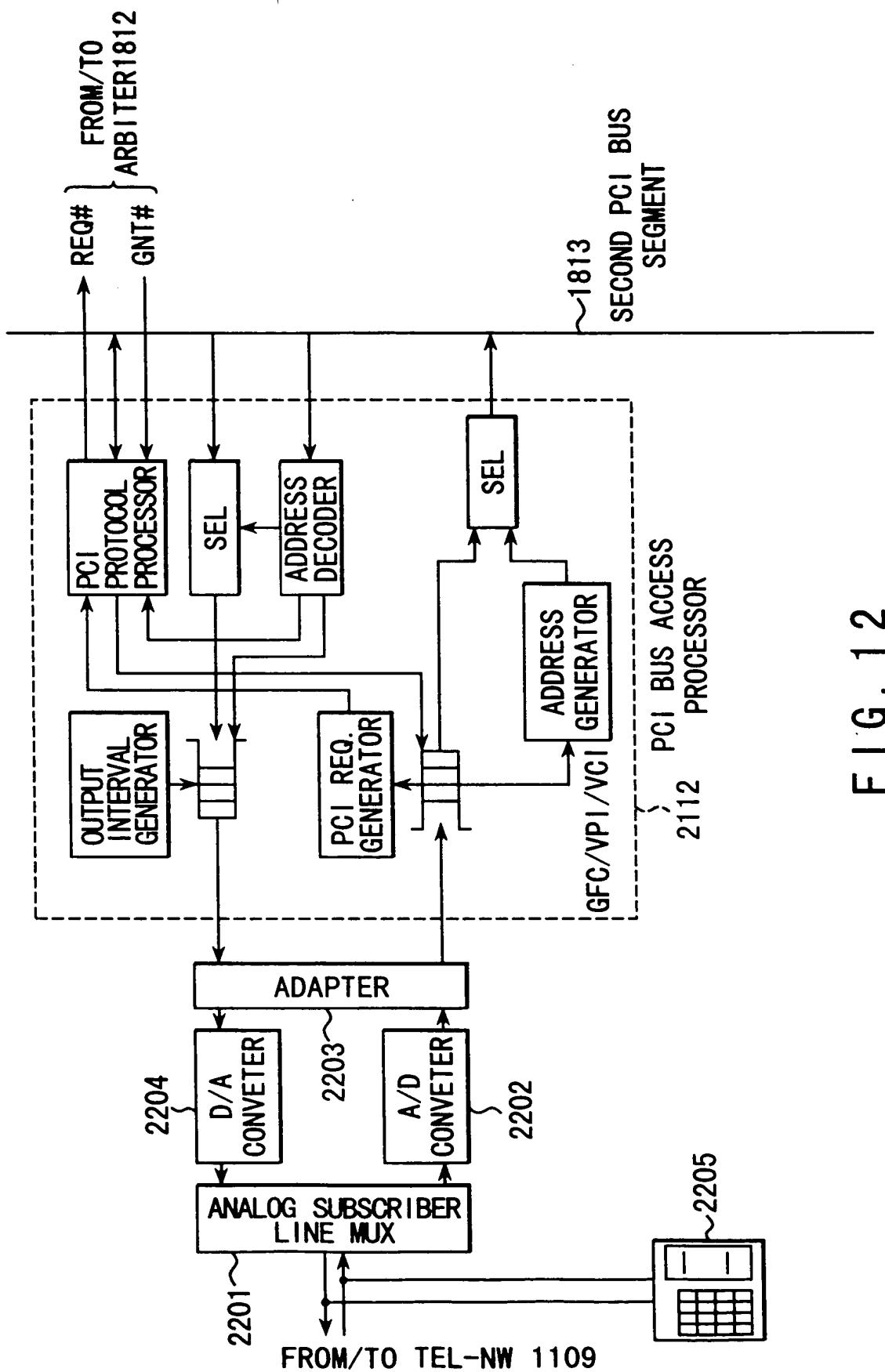
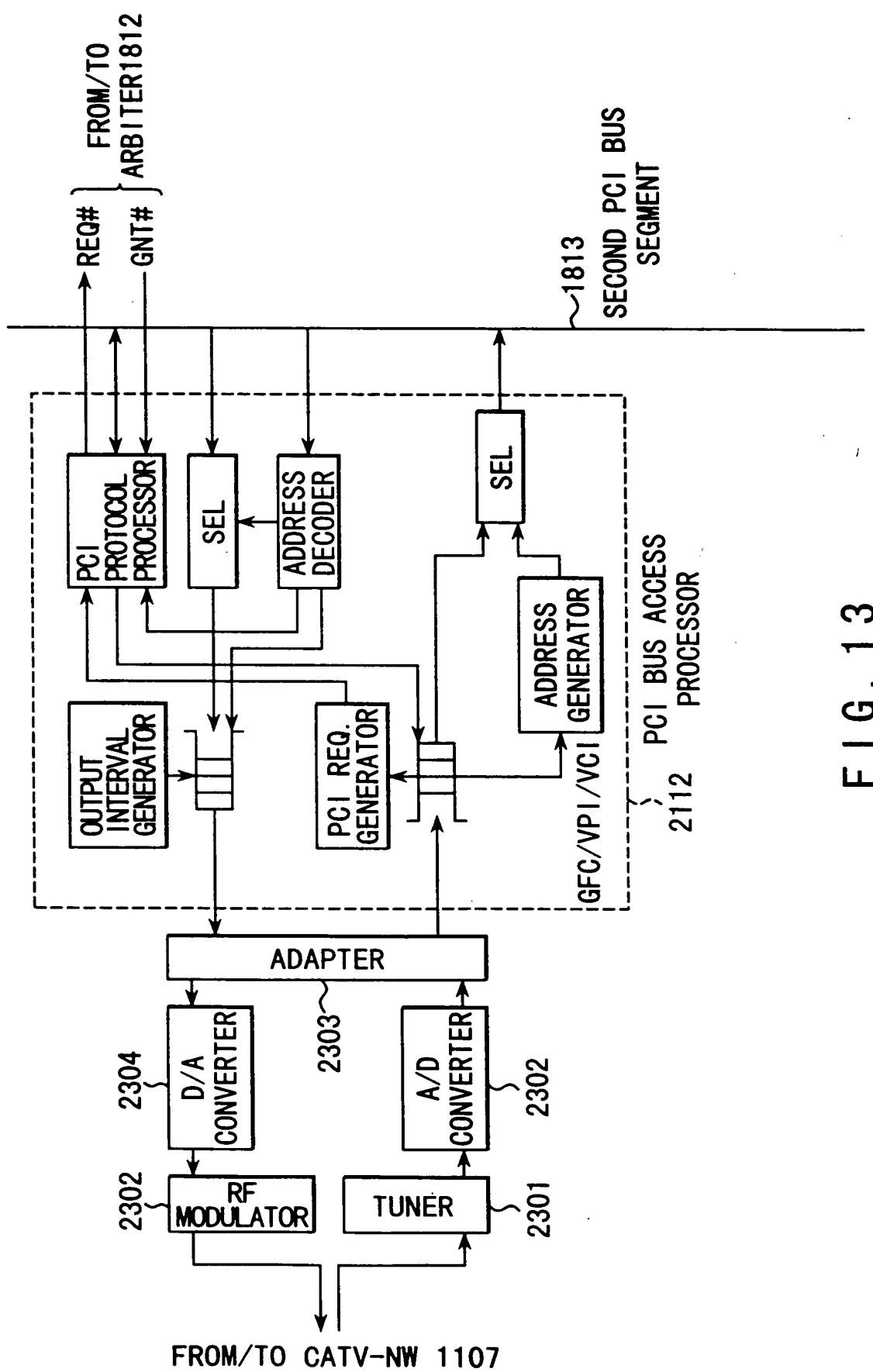


FIG. 12



3
—
E
—
G.

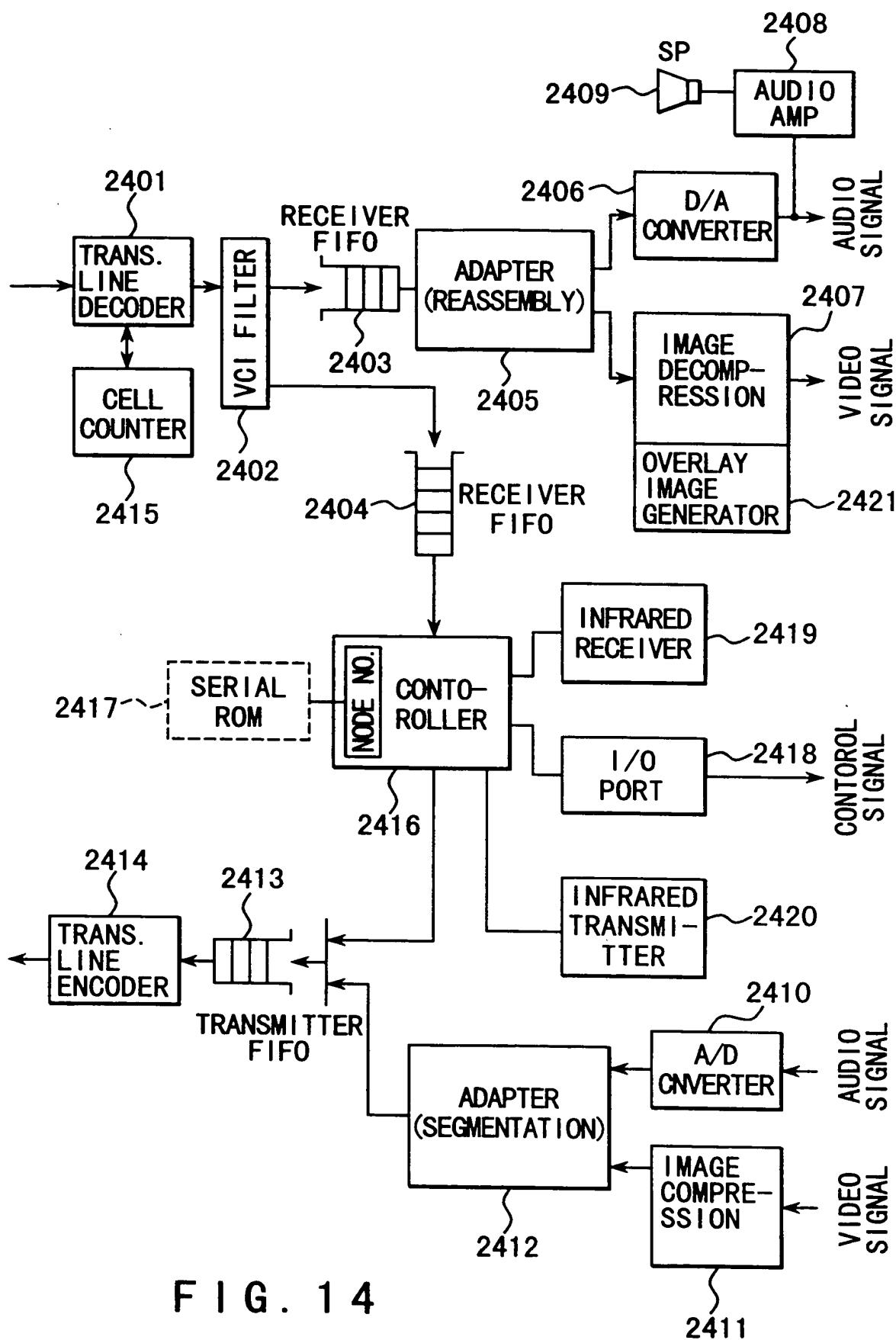
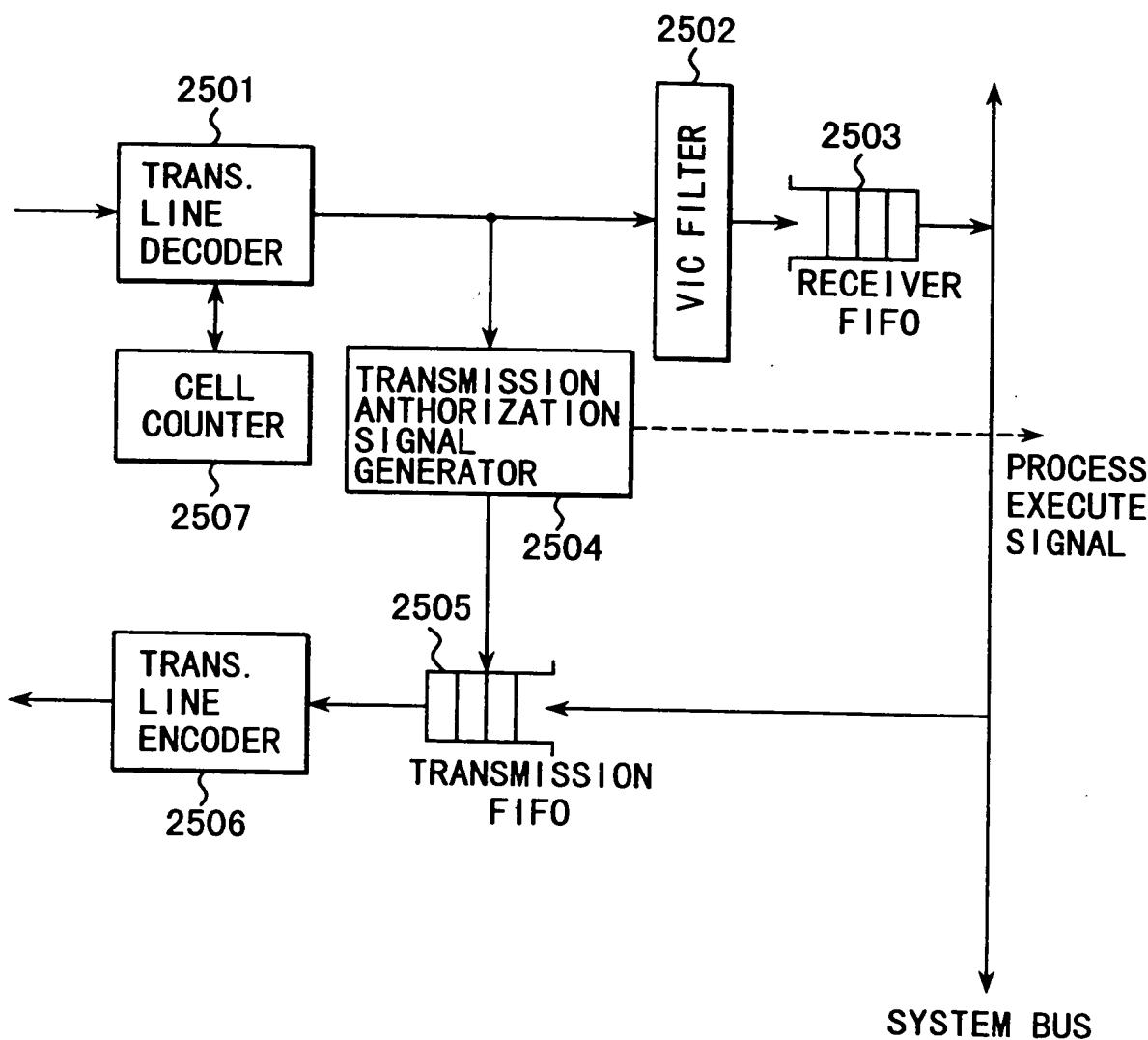


FIG. 14



F I G . 1 5

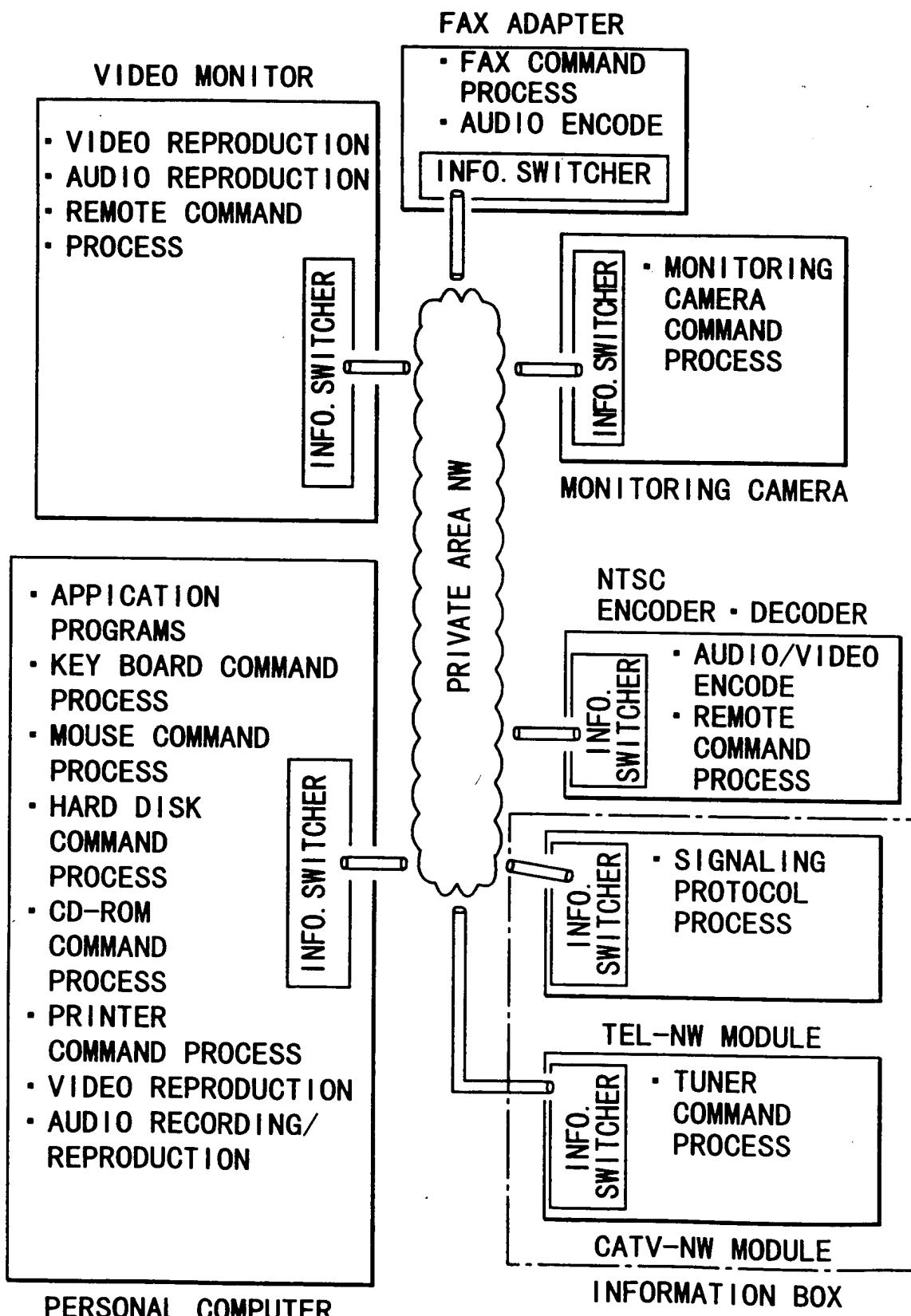


FIG. 16